We claim:

1. A method of processing data for defining a layer in an integrated circuit which is outputted to form a set of phase and trim masks comprising:

(a) loading into layout processing software the GDS data for two layers that define a transistor, preferably, for diffusion (active area) and polysilicon gate layers.

(b) generating a phase mask by checking alt-PSM design rules for phase conflict, assigning full size scattering bars (FSSB) for small linewidths, assigning phases with a constant phase width along the gate area, resizing FSSB on field oxide, and generating optical proximity corrections which are then inputted into the design,

(c) inputting gate block data that includes assigned phase areas and polygate areas (true gate) to prevent erasure of shrunken gates,

(d) generating a trim mask by inputting parameters that define interconnect features (poly layer excluding gates), block area data from (c), and sub-resolution scattering bar information, and generating optical proximity corrections which are then inputted into the design, and

(e) providing a modified GDS layout for each mask for mask fabrication.

2. The method of claim **1** wherein said layout processing software is commercially available EDA IC design software or a set of script programs.

3. The method of claim **1** wherein said alt-PSM design includes a set of parameters for perpendicular gate, inter-digital gate, poly to poly pitch, and line-end cap.

4. The method of claim **1** wherein the said phase assignment includes rules for the parameters of phase width, minimum phase width, phase spacing, phase extension, and overlay shift.

5. The method of claim **1** wherein said optical proximity correction means said layout is modified according to rule based or empirical resist model based data such that the printed pattern is close to the intended design in the original IC layout.

6. The method of claim **1** wherein said trim mask is a tritone mask comprised of chrome regions to protect shrunken gate areas, attenuated phase regions for defining interconnects, and transparent regions.

7. The method of claim **1** wherein said sub-resolution scattering bars are defined by parameters including size, separation from interconnect features, and number of scattering bars along each interconnect feature in the trim mask layout.

8. The method of claim **7** wherein from one to three scattering bars are included along each interconnect line in the trim mask layout and said bars have a width from between 33% and 100% of the width of the interconnect line and are separated from said interconnect line by a distance from one to two times the width of an interconnect line.

9. The method of claim **1** wherein from one to three full size scattering bars are positioned between chrome lines that are used to define shrunken gates and each scattering bar separates a θ^{o} phase region from a $(180 + \theta)^{o}$ phase region.

10. The method of claim **9** wherein the width of said scattering bars is equal to or greater than the width of said chrome lines that define the shrunken gates and the phase widths of transparent regions adjacent to said chrome lines that define shrunken gates are the same as the phase widths adjacent to said scattering bars.

11. A method for producing phase shifting layout data by a command script system that applies alt-PSM design rules, OPC, scattering bar rules, and gate blocking area generation comprising:

(a) identifying a single line transistor gate in an integrated circuit,

(b) defining phase shifting areas for an alternating phase shifting mask (alt-PSM), said phase mask including said single line transistor gate and first opaque areas,

(c) providing a layout including phase shifting areas in an opaque field and another layout of phase θ^{O} or phase $(180 + \theta)^{O}$ for said alt-PSM wherein θ is from 0 to 180,

(d) assigning phase areas and polygate areas (true gate) for a gate block layer,

(e) providing a layout for a tritone attenuated phase shift mask (att-PSM) including interconnects (poly layer excluding gates), block area from (d), and sub-resolution scattering bars , and

(f) processing the layouts for optical proximity corrections and outputting a modified GDS layout for mask fabrication.

12. The method of claim **11** wherein said phase mask is designed with a gate having a width and a length, said length is orthogonal to the two longer sides of an underlying active area layer, and said length is longer than the width of said active area.

13. The method of claim **11** wherein the alternating phase shifting areas include a set of θ^{O} phase and $(180 + \theta)^{O}$ phase regions, and each gate feature is adjacent to one θ^{O} phase region and one $(180 + \theta)^{O}$ phase region.

14. The method of claim **13** wherein the phase shifting areas are comprised of chrome regions positioned between a θ^{O} phase region and $(180 + \theta)^{O}$ phase region.

15. The method of claim **11** wherein from one to three full size scattering bars are positioned between chrome lines that are used to define shrunken gates and each scattering bar separates a θ^{O} phase region from a $(180 + \theta)^{O}$ phase region.

16. The method of claim **15** wherein the width of said scattering bars is equal to or greater than the width of said chrome lines that define the shrunken gates and the phase widths of transparent regions adjacent to said chrome lines that define shrunken gates are the same as the phase widths adjacent to said scattering bars.

17. The method of claim **11** wherein said transistor gate comprises a single, substantially straight line in said layout.

18. The method of claim **11** wherein said opaque gate block area includes phase shifting areas on the phase layout and polygate on active area and the size of said gate block area is demagnified somewhat on phase layouts to compensate for possible misalignment between first (alt-PSM) and second (att-PSM) masks.

19. The method of claim **11** wherein said attenuated regions in said att-PSM are used to define interconnect features having a width larger than said gate width.

20. The method of claim **19** wherein the scattering bars have a width from between 33% and 100% of the interconnect feature width and are separated from an interconnect feature by a distance that is from 1 to 2 times the width of said interconnect feature.

21. A method for simultaneously producing a gate feature and an interconnect feature in an integrated circuit which have linewidths smaller than can be achieved by conventional methods comprising:

(a) providing a substrate which is coated with a positive tone photoresist layer,

(b) exposing said photoresist with a first mask comprised of alternating phase shift regions separated by chrome regions,

(c) exposing said photoresist with a second mask comprised of attenuated phase shift regions that define interconnect features, chrome block regions that protect shrunken gates defined in the first exposure, and clear transparent regions,

(d) developing said photoresist layer on said substrate, and

(e) transferring the pattern formed in the photoresist through the underlying substrate with a dry etch process.

22. The method of claim **21** wherein the mask substrate is quartz or CaF_2 and the exposing radiation is selected from one or more wavelengths in a range from about 150 nm to about 600 nm.

23. The method of claim **21** wherein the linewidths in the printed photoresist pattern are between ¼ and ½ of the exposing wavelength in size.

24. The method of claim **21** wherein the substrate is polysilicon.

25. The method of claim **21** wherein from one to three full size scattering bars are positioned between chrome lines that are used to define shrunken gates on said alternating phase shifting mask and each scattering bar separates a θ^{o} phase region from a $(180 + \theta)^{o}$ phase region wherein θ is from 0 to 180.

26. The method of claim **25** wherein the width of said scattering bars is equal to or greater than the width of said chrome lines that define the shrunken gates and the phase widths of transparent regions adjacent to said chrome lines that define shrunken gates are the same as the phase widths adjacent to said scattering bars.

27. The method of claim **21** wherein said attenuated phase regions are comprised of a half-tone material such as $MoSiO_XN_Y$ which has been deposited on a transparent substrate.

28. The method of claim **27** wherein the said attenuated phase regions transmit from about 1% to 30% of incident light and phase shift said light by 180^O relative to light that is transmitted through transparent regions that are not phase shifted.

29. The method of claim **27** wherein the attenuated regions contain from one to three scattering bars that are used to define a smaller interconnect feature than is possible with conventional attenuated phase shifting.

30. The method of claim **29** wherein the width of the scattering bars is between 33% and 100% of the interconnect feature width and said bars are separated from said interconnect by a distance that is from one to two times the width of said interconnect.

31. The method of claim **21** wherein the exposed photoresist layer is developed with an aqueous base solution.

32. A method of forming a feature on a substrate that includes a first exposure with an alternating phase shift mask with full size scattering bars and a second exposure with a tritone attenuated mask having at least one scattering bar, said scattering bars are not printed in the resulting pattern from the lithography process.